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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,223	09/30/2003	Lei Ding	29250-001081/US	1580
7590 HARNESS, DICKEY & PIERCE, P.L.C. P.O. Box 8910 Reston, VA 20195			EXAMINER LEE, SIU M	
		ART UNIT 2611	PAPER NUMBER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/673,223	DING ET AL.	
	Examiner	Art Unit	
	Siu M. Lee	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 13 March 2007.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1,2,4,7-10,13-19 and 22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,2,4,7-10,13-19 and 22 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 31 March 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Remarks

1. Applicant's arguments, see page 8, filed 3/13/2007, with respect to "CLAIM OBJECTIONS" have been fully considered and are persuasive. The objection of Claim 8 has been withdrawn.
- 2.
3. Applicant's arguments with respect to claims 1, 2, 4, 7-10, 13-19, and 22 on page 8-10, filed 3/13/2007 have been fully considered but they are not persuasive.

Applicant's argument:

The reference, Wright et al. (US 5,990,734) fails to suggest or teach a compensator constructor estimating cross coupling channels between in-phase and quadrature phase components.

Examiner's response:

Wright et al. (US 5,990,734) discloses an adaptive control processing and compensation estimator (ACPCE) 28 in figure 14 wherein the ACPCE comprises a parallel numerical model (model LINC amplifier) 143 to mirror the expected processes of the real analog LINC amplifier 20, including the analog chains (upconversion 23 and 24). Figure 16 is the schematic diagram of the LINC model amplifier 143, wherein the LINC model amplifier 143 comprises quadrature modulator compensation 161 and 162. The schematic diagram of the quadrature modulator compensator 161 and 162 is shown in figure 19. The quadrature modulator compensator compensates the IQ crosstalk correction that takes the one channel (in this case Q channel but the inverse

arrangement is a valid alternative) and scales it before adding it to the other channel. The examiner interpret this IQ crosstalk correction as a cross coupling between the in-phase and quadrature phase components and therefore satisfy the claim limitation.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 4, 13, 17, 18, 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Wright et al. (US 5,990,734).

- (1) Regarding claim 1:

Wright et al. discloses an amplifier to be used in a transmitter (figure 2, column 7, lines 39-43) comprising an upconverter (upconverter (RF upconversion) 23 or 24 in figure 2, column 7, lines 46-47) for converting one frequency signal to another frequency signal (column 10, lines 10-18); and a compensator including a filter unit (digital compensation signal processor (DCSP) 21 in figure 9 contains FIR filter 92 and 93, column 17, lines 45-48) for compensating at least one of gain distortion and phase distortion introduced into the one frequency signal by at least the upconverter (all the distortion introduced to the component signals by the analog chains including amplifier, baseband filtering, and RF upconversion are modeled and compensate by the digital compensation signal processor (DCSP) 21) (column 18, lines 7-17, column 26, lines 37-

42), the one frequency signal including in-phase components and quadrature phase components (FIR filter 92 is used to correct for gain and phase rotation characteristics of the analog circuits, the FIR filter has an input $x(t)$, which is a complex value made up of an I and a Q component) (column 18, lines 30-35); and

a compensator constructor (adaptive control processing and compensation estimator (ACPCE) 28 in figure 2), based on a channel model of at least the direct upconverter (fig 16 depicts a mathematical model structure that may be used to model the analog chain including the upconverter, column 26, lines 35-42) that includes an in-phase channel, a quadrature phase channel and cross coupling channels between the in-phase and quadrature phase channels (quadrature modulator compensation 161 and 162 in figure 19 contain an I channel $I(t)$ correction, a Q channel $Q(t)$ correction and a IQ crosstalk correction), estimating the in-phase channel, the quadrature phase channel, and the cross coupling channels between the in-phase and quadrature phase components (the I and Q channel is being scale by the correction coefficient to correct for the gain imbalance, DC+LO offset, the IQ crosstalk correction (cross coupling) take one channel (in this case the Q channel but the inverse arrangement is a valid alternative) and scale it before adding it to the other channel) and constructing filters in the filter unit based on the estimates (the third stage of the system identification is used to identify the imperfections of the LINC amplifier by adjusting the parameters of the parallel numerical model such that the observed amplifier output and predicted amplifier output are substantially identical. Once this has been achieved the parameters of the

numerical model may be used to compute the initial compensation parameters of the digital compensation signal processing block 21, column 24, line 60-column 25, line1).

(2) Regarding claim 2:

Wright et al. discloses an amplifier to be used in a transmitter wherein the upconverter (upconverter 23 and 24 in figure 2, column 7, lines 46-47) is a direct upconverter for directly upconverting a baseband signal to an RF signal (direct conversion from complex baseband signal to radio frequency signal) (column 10, lines 10-18); and the compensator (digital compensation signal processor (DCSP) 21 in figure 2) compensates for at least one of gain imbalance and phase imbalance introduced into the baseband signal by at least the direct up converter (column 18, lines 7-17).

(3) Regarding claim 4:

Wright et al. discloses an amplifier to be used in a transmitter wherein the compensator (digital compensation signal processor (DCSP) 21 in figure 2) compensates for dc offset introduced into the baseband signal by at least the direct upconverter (column 18, lines 7-17, column 26, lines 37-42).

(4) Regarding claim 13:

Wright et al. further discloses an amplifier to be used in a transmitter wherein the compensator compensates for dc offset introduced into the lower frequency signal by at least the upconverter (figure 10B the I channel DC offset correct and the Q DC offset correct compensate for the DC offset introduced by the analog chain, column 18, lines 58-61).

(5) Regarding claim 17:

Wright et al discloses a method of generating RF signal comprising up converting one frequency signal to another frequency signal (upconvert baseband signal to radio frequency signal by the RF conversion 23 and 24 in figure 2) (column 10, lines 10-18); and compensating using a filter unit for at least one of gain and phase distortion introduced into the one frequency signal by at least the upconversion (the digital compensation signal processor 21 in figure 2 compensates the at least one of gain and phase distortion introduced into the one frequency signal by at least the upconversion) (column 9, lines 29-36), the one frequency signal including in-phase components and quadrature phase components (FIR filter 92 is used to correct for gain and phase rotation characteristics of the analog circuits, the FIR filter has an input $x(t)$, which is a complex value made up of an I and a Q component) (column 18, lines 30-35);

deriving, based on a channel model of at least the upconverting step (fig 16 depicts a mathematical model structure that may be used to model the analog chain including the upconverter, column 26, lines 35-42) that includes an in-phase channel, a quadrature phase channel and cross coupling channels between the in-phase and quadrature phase channels (quadrature modulator compensation 161 and 162 in figure 19 contain an I channel $I(t)$ correction, a Q channel $Q(t)$ correction and a IQ crosstalk correction), estimates of the in-phase channel, the quadrature phase channel, and the cross coupling channels between the in-phase and quadrature phase components (the I and Q channel is being scale by the correction coefficient to correct for the gain imbalance, DC+LO offset, the IQ crosstalk correction (cross coupling) take one channel

(in this case the Q channel but the inverse arrangement is a valid alternative) and scale it before adding it to the other channel);

and constructing filters in the filter unit based on the estimates (the third stage of the system identification is used to identify the imperfections of the LINC amplifier by adjusting the parameters of the parallel numerical model such that the observed amplifier output and predicted amplifier output are substantially identical. Once this has been achieved the parameters of the numerical model may be used to compute the initial compensation parameters of the digital compensation signal processing block 21, column 24, line 60-column 25, line1).

(6) Regarding claim 18:

Wright et al. discloses a method further comprising compensating for dc offset introduced into a lower frequency signal by at least the upconversion (the digital compensation signal processor 21 in figure 2 compensates for the DC offset introduced in the analog chain including the RF upconversion) (column 9, lines 29-36).

(7) Regarding claim 19:

Wright et al. disclose a method wherein the up converting step directly up converts a baseband signal to the RF signal (column 10, lines 10-18).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wright et al. (US 5,990,734) in view of Zhang (US 6,687,311 B1) and Birru (US 2002/0037058 A1).

Wright et al. discloses an amplifier to be used in a transmitter wherein the compensator constructor (adaptive control processing and compensation estimator (ACPCE) 28 in figure 2) derives the filters as an inverse of the channel model for the analog chain including the upconverter, which represents a mean squared error (Least mean square algorithm that minimize the root mean square value, column 28, lines 12-20), in the frequency domain (frequency dependent amplitude, delay and phase ripple can be modeled, column 27, lines 1-2), between a desired response of a system including at least the direct upconverter ($S_{predicted}(t)$) represent the calculated equivalent of the output, column 26, lines 55-56) and an actual response of the system including at least the filters and the direct upconverter ($S_{obs}(t)$) represent the observed power amplifier output from the analog chain including the upconverter, column 27, lines 17-21) (equation 8 in column 27, line 51 represent the difference between the observed recombined signal sampled from the analog down conversion and the executed output that was predicted by the LINC model used for system identification, column 27, lines 62-65)..

Wright et al. fails to disclose; (a) derives the inverse of the channel model derived from a cost function and (b) derives the filters as an inverse of the channel model for the direct upconverter.

With respect to (a), Birru discloses the inverse of the channel model derived from a cost function (claim 11 in page 6, Birru discloses a frequency domain equalizer that calculate the frequency domain inverse channel estimate utilizing a least square cost function).

It is desirable to calculate the inverse of the channel model derived from a cost function in frequency domain because it is a more cost-effective solution (paragraph 0059, lines 5-6). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teaching of Birru with the system of Wright et al. to reduce the cost of the system.

With respect to (b), Zhang discloses a system that derives an inverse of the channel model for the direct upconverter (column 3, lines 55-60).

It is desirable to derive an inverse of the channel model for the direct upconverter because the complexity and cost of the system is substantially reduced, thereby resulting in significant savings (column 5, lines 55-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Zhang in the system of Wright et al. to reduce the manufacturing cost of the system.

3. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wright et al. (US 5,990,734) in view of Zhang (US 6,687,311 B1).

(1) Regarding claim 8:

Wright et al. discloses an amplifier to be used in a transmitter wherein the compensator constructor estimates each of the of the in-phase channel (the I channel

$I(t)$ in figure 19), the quadrature phase channel (the Q channel $Q(t)$ in figure 19), and the cross coupling channels between the in-phase and quadrature phase channels (IQ crosstalk correction in figure 19) based on output from a analog chain including the upconverter and the amplifier.

Wright et al. fails to disclose the compensator constructor estimations are based on output from the compensator and a baseband signal derived from output of the direct upconverter.

However, Zhang discloses a system comprising a compensator constructor estimations (monitor 240 in figure 2 monitors the amplitude and phase of the RF signal and provides corresponding amplitude and phase adjustment information to the equalizer 207 via a feedback path 245, column 3, lines 55-60) based on output from the compensator (digital filter 205 in figure 2) and a baseband signal derived from output of the direct upconverter (RF driver 230 in figure 2)..

It is desirable to derive an inverse of the channel model for the direct upconverter because the complexity and cost of the system is substantially reduced, thereby resulting in significant savings (column 5, lines 55-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Zhang in the system of Wright et al. to reduce the manufacturing cost of the system.

(2) Regarding claim 9:

Wright et al discloses an amplifier to be used in a transmitter comprising a feedback path including a down converter (RF down converter 26 in figure 2) down converting output of the analog chain and wherein the compensator constructor

(adaptive control processing and compensation estimator (ACPCE) 28 in figure 2) receives a signal on the feedback path.

Wright et al fails to disclose a feedback path from the output of the direct upconverter.

However, Zhang teaches a system that comprises a feedback path (feedback path 245 in figure 2, column 3, lines 59-60) from the output of the direct upconverter (the direct QAM modulator 200 in figure 2 does not use an IF stage, therefore, it is using a direct upconverter RF driver 230 in figure 2, column 3, lines 61-63).

It is desirable to employ the teaching of Zhang with the system of Wright et al. because the complexity and cost of the system is substantially reduced, thereby resulting in significant savings (column 5, lines 55-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Zhang in the system of Wright et al. to reduce the manufacturing cost of the system.

(3) Regarding claim 10:

Wright et al. discloses a amplifier to be used in a transmitter further comprising a power amplifier (amplifier 15 and 16 in figure 2, column 8, lines 43-45) amplifying the RF signal for transmission (amplifiers 15 and 16 are connected to the output of the RF upconverter 23 and 24 in figure 2); a feedback path including a down converter (RF down conversion 26 in figure 2) down converting output of the power amplifier; and wherein the compensator constructor (adaptive control processing and compensation estimator (ACPCE) 28 in figure 2) receives a signal on the feedback path.

4. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wright et al. (US 5,990,734) in view of Poklemba et al. (US 2003/0141938 A1).

(1) Regarding claim 14:

Wright et al. discloses a transmitter comprising:

a direct upconverter (upconverter 23 or 24 in figure 2, column 7, lines 46-47) for converting a baseband signal directly to an RF signal (column 10, lines 10-18), the baseband signal including in-phase and quadrature phase components (the input signal to the upconverter ($Ph_{Adc}(t)$ and $Ph_{Bdc}(t)$) are complex baseband signals that consist of a real and imaginary components) (column 10, lines 11-13);

a first filter for filtering the in-phase component to compensate for at least one of gain imbalance and phase imbalance in the in-phase component (the modulator 94 and 95 is similar to the FIR filter, column 18, lines 66-67) (the I channel gain imbalance in figure 10B, column 18, lines 58-61);

a second filter for filtering the quadrature phase component to compensate for at least one of gain imbalance and phase imbalance in the in-phase component associated with cross-coupling of the quadrature phase component with the in-phase component (the IQ crosstalk correction 109 in figure 10B, column 18, lines 58-61);

a third filter for filtering the quadrature phase component to compensate for at least one of gain imbalance and phase imbalance in the quadrature phase component (Q channel gain imbalance in figure 10B, column 18, lines 58-61); and

Wright et al. fails to discloses a fourth filter for filtering the in-phase component to compensate for at least one of gain imbalance and phase imbalance in the quadrature

component associated with cross-coupling of the in-phase component with the quadrature component.

However, Poklemba et al discloses a modulator cross coupled arm filters (filters 14, 16, 18, 20 in figure 1, paragraph 0039, lines 20-23) comprising a filter (filter 16 in figure 1) for filtering the in-phase component (input from quadrature data mapper 12 in figure 1) to compensate for at least one of gain imbalance and phase imbalance in the quadrature component associated with cross-coupling of the in-phase component with the quadrature component (paragraph 0039, lines 25-36).

It is desirable to discloses a fourth filter for filtering the in-phase component to compensate for at least one of gain imbalance and phase imbalance in the quadrature component associated with cross-coupling of the in-phase component with the quadrature component because it is more efficient in bandwidth and SNR than conventional transmission technique (paragraph 0081, lines 11-13). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teaching of Poklemba et al. with the system of Wright et al. to improve the signal quality of the system.

(2) Regarding claim 15:

Wright et al. discloses the direct upconverter (RF upconverter 23 and 24 in figure 2) receives output from the first and second adders (the adders from the filter in digital compensation signal processor (DCSP) 21 in figure 2).

Wright et al fails to disclose a first adder adding output of the first and second filters; a second adder adding output of the third and fourth filters.

Poklemba et al. further discloses a first adder (adder 22 in figure 1) adding output of the first and second filters (paragraph 0040, lines 1-7); a second adder (adder 24 in figure 1) adding output of the third and fourth filters (paragraph 0040, lines 1-7).

It is desirable to have a first adder adding output of the first and second filters; a second adder adding output of the third and fourth filters because it is more efficient in bandwidth and SNR than conventional transmission technique (paragraph 0081, lines 11-13). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teaching of Poklemba et al. with the system of Wright et al. to improve the signal quality of the system.

(3) Regarding claim 16:

Wright et al. further discloses a third adder (adder in I channel DC offset correct in figure 10B) adding a first dc offset to the in-phase component to compensate for dc offset introduced into the baseband signal by at least the direct upconverter (compensate for baseband DC offset imperfection of the IQ modulator including the upconverter, column 18, lines 58-61); and a fourth adder (adder in Q channel offset correct in figure 10B) adding a second dc offset to the quadrature phase component to compensate for dc offset introduced into the baseband signal by at least the direct upconverter (compensate for baseband DC offset imperfection of the IQ modulator including the upconverter, column 18, lines 58-61); and wherein the direct upconverter receives output from the third and fourth adders (the RF upconversion 23 and 24 in figure 2 receive output from the digital compensation signal processor (DCSP) 21 in figure 2).

5. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wright et al. (US 5,990,734) in view of Birru (US 2002/0037058 A1).

Wright et al. discloses an amplifier to be used in a transmitter comprising an upconverter for converting one frequency signal to another frequency signal (upconverter 23 or 24 in figure 2 converts a baseband signal directly to an RF signal, column 7, lines 46-47, column 10, lines 10-18); and a compensator includes at least one filter modeled (the tap coefficients have been updated by the adaptive control processing and compensation estimator (ACPCE) 28, column 18, lines 44-47) (FIR filter in figure 10A, column 18, lines 35-42) as an inverse of a channel model (column 26, lines 61-65) for at least the upconverter (the FIR filters in figure 16 is a mathematical model of the of the analog chain including the upconverter, column 26, lines 61-65), which represents a mean squared error (Least mean square algorithm that minimize the root mean square value, column 28, lines 12-20), in the frequency domain (frequency dependent amplitude, delay and phase ripple can be modeled, column 27, lines 1-2) ,between a desired response of a system including at least the upconverter ($S_{predicted}(t)$) represent the calculated equivalent of the output, column 26, lines 55-56), and an actual response of the system including at least the filter and the upconverter ($S_{obs}(t)$) represent the observed power amplifier output from the analog chain including the upconverter, column 27, lines 17-21) (equation 8 in column 27, line 51 represent the difference between the observed recombined signal sampled from the analog down conversion

and the executed output that was predicted by the LINC model used for system identification, column 27, lines 62-65).

Wright et al. fails to disclose the inverse of the channel model derived from a cost function.

However, Birru discloses the inverse of the channel model derived from a cost function (claim 11 in page 6, Birru discloses a frequency domain equalizer that calculate the frequency domain inverse channel estimate utilizing a least square cost function).

It is desirable to calculate the inverse of the channel model derived from a cost function in frequency domain because it is a more cost-effective solution (paragraph 0059, lines 5-6). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teaching of Birru with the system of Wright et al. to reduce the cost of the system.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Siu M. Lee whose telephone number is (571) 270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Siu M. Lee

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Examiner
Art Unit 2611
5/22/2007

Chieh M. Fan
CHIEH M. FAN
SUPERVISORY PATENT EXAMINER